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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,836	06/17/2001	Brian Bailey	1011-64537-01	9966

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KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2121	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	09/883,836	BAILEY ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4,6-22,24-31,34 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,6-22 and 24-31* is/are allowed.

6)☒ Claim(s) *34 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/17/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 4,6-22,24-31,34 and 37.

Section I: Non-Final Rejection

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 34 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Bortfeld (US Patent 6,993,469; hereafter Bortfeld). Bortfeld teaches an improvement of co-simulation of circuits (abstract).

Claim 34. A method comprising: simulation a first abstraction level (different abstraction levels, (figure 1 with column 5, lines 31-39) of a circuit functionality in a circuit design (electronic design automation, column 1, lines 20-24)with a first simulation model

(teaches a first plurality of activities based within a simulation environment, column 20, lines 50-53) in an electronic design automation (EDA) simulation environment; simulating a second abstraction level (figure 1 with column 5, lines 31-39) of the circuit functionality in the circuit design (electronic design automation, column 1, lines 20-24)with a second simulation model (teaches a second plurality of activities based within a simulation environment, column 20, lines 50-55) in the EDA simulation environment (column 1, lines 20-25 and column 20, line 52), wherein the first simulation model (teaches a first plurality of activities based within a simulation environment, column 20, lines 50-53) and the second simulation model (teaches a second plurality of activities based within a simulation environment, column 20, lines 50-55) are among a plurality of simulation models (encompasses the simulation environment, column 1, lines 20-25 and column 20, line 52) representing a same functionality in the circuit design, each of the plurality of simulation models having a particular level of performance and resolution, and each of the plurality of simulation models (encompasses the simulation environment, column 1, lines 20-25 and column 20, line 52) being used at different stages of simulation depending on a desired performance level and/or resolution level of the simulation; reading state information (column 3, lines 53-55)from the first simulation model (teaches a first plurality of activities based within a simulation environment, column 20, lines 50-53) in the EDA simulation environment (column 1, lines 20-25 and column 20, line 52) when a simulation domain (encompasses the simulation environment, column 1, lines 20-25 and column 20, line 52) of the first simulation model (teaches a first plurality of activities based within a simulation environment, column 20,

lines 50-53) is deactivated; and writing the state information (column 3, lines 53-55)to the second simulation model (teaches a second plurality of activities based within a simulation environment, column 20, lines 50-55) in the EDA simulation environment (column 1, lines 20-25 and column 20, line 52) prior to activation of a simulation domain (encompasses the simulation environment, column 1, lines 20-25 and column 20, line 52) of the second simulation model (teaches a second plurality of activities based within a simulation environment, column 20, lines 50-55).

Claim 37. The method of claim 4 wherein simulating the transfer (column 5, lines 58-61)from the first simulation model to the second simulation model (teaches a second plurality of activities based within a simulation environment, column 20, lines 50-55) in the circuit design (electronic design automation, column 1, lines 20-24)comprises transferring the \state information (column 3, lines 53-55)through at least one additional simulation model in the EDA simulation environment (column 1, lines 20-25 and column 20, line 52).

Allowable Subject Matter

4. Claims 4,6-22,24-31 stand allowed.

5. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Section II: Response to Arguments

Claim Objections

6. Applicants are thanked for addressing these issues. Applicants have clarified and confirmed that the first and second simulation models as any simulation model with access to the coherent state storage can exchange state information (column 3, lines 53-55)with any other simulation model... (see applicants' response, pg. 9 of 11, 3rd paragraph and the first and second hardware components are models a USB bus to connect the peripheral to another hardware component. Objections are withdrawn.

Claim Rejections 112/102(e)

7. Applicants are thanked for addressing these issues. Rejections are withdrawn. However a new rejection is completed for claims 34 and 37 as set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- US Patent 7,050,956 teaches a method predicts performance of a system that includes a plurality of interconnected components defining at least one data flow path. The method references a workload specification for the system. The method models the system using one or more component models.

- US 6993469 B1 teaches a significant improvement over current methods for co-simulation of the hardware and software components of embedded digital system designs is provided. The present invention integrates the hardware and software components of a system design into a single unified simulation environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. David Vincent 571-272-3080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

12/6/07

David Vincent
Supervisory Patent Examiner
Tech Center 2100